Hall Effect

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Semiconductors have changed the way the world works and computes. By changing these elements through doping processes, the electrical properties of the material change, opening a variety of use cases including measuring magnetic fields. Electrical properties of a silicon wafer with an unknown dopant was measured. The type of dopant was found to be p-type using the thermoelectric effect and the Hall effect. The resistivity of the wafer was found using the 4-wire approach to be 6.03±0.9 Ohm-cm compared to a typical value of 6.40 Ohm-cm. P-type silicon semiconductors have a typical carrier concentration between 10^{13} and $3 * 10^{18} cm^{-3}$. This experiment calculated a carrier concentration of $(1.90 \pm 0.10) * 10^{15} cm^{-3}$ which is well within typical values. From this carrier concentration, a typical resistivity and carrier mobility are 7.97 Ohm-cm and $412.2 \frac{cm^2}{V-s}$, respectively. The values found were 6.3 ± 0.9 Ohm-cm and $520 \pm 80 \frac{cm^2}{V-s}$ which agrees with the values found in literature.

INTRODUCTION

Semiconductors are used in various industries and have revolutionized computing in the past century. Silicon is the most widely used material in the semiconductor industry since it is cheap, abundant, and very efficient. To make semiconductors more useful, they are doped with a material that has either one less or one more electron in its valence shell than silicon. These correspond to p-type and n-type semiconductors, respectively. By using the thermoelectric effect or the Hall effect, one can tell if a sample is n-type or p-type.

The Hall effect is a result of when a charge is moving with a velocity in a magnetic field. A Lorentz force will be applied to the charge according to Equation 1 where q is the charge of the particle, F is the force being applied, v is the velocity of the particle, and B is the magnetic field. This effect is very useful when trying to measure a magnetic field. By putting a semiconductor in a magnetic field and measuring the voltage produced from this force, one can calculate the magnetic field.

$$F = q(v \times B) \tag{1}$$

APPARATUS

The apparatus consisted of the following.

- Doped silicon wafer
- Pre-wired circuit board
- Carbide scriber
- Soldering Iron/Indium Solder
- Power Supply, GPS-3030DD
- GMW Electromagnet, Model 3470

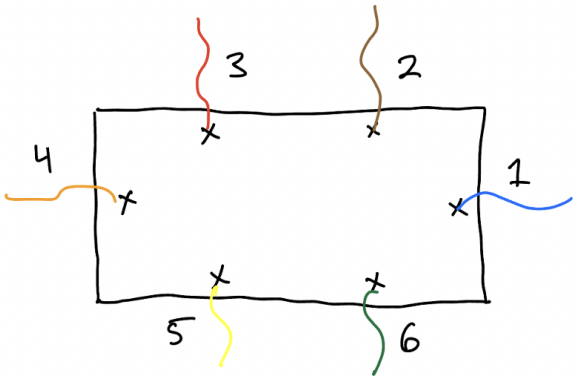

FIG. 1. Silicon Wafer Set-up with Labeled Nodes

- 2 DMM's
- FW Bell Gauss meter, Model 5070

PROCEDURES AND RESULTS

A. Silicon Wafer Set-up

The experiment was started by soldering 6 wires onto a doped silicon wafer using indium solder. When silicon is left out, a silicon oxide layer is formed on the outside. To improve connectivity of the wires, a carbide sciber was used to scratch the outside layer off at a small node for each wire. The orientation of the wires and their corresponding labeled nodes can be seen in Figure 1. The silicon sample was previously glued onto a circuit board with a small amount of rubber cement. It is important to note that when soldering the wires onto the wafer, the soldering iron was not touching the chip for more than a few seconds. This is because the iron did not have temperature control and it could burn the wafer if it was held there for longer.

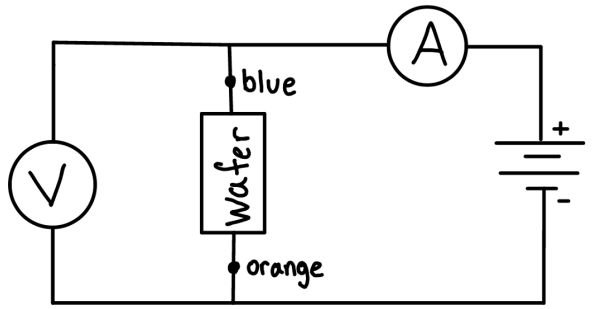

FIG. 2. Circuit Diagram for Initial Set-up

Once all the wires were soldered, a DMM was used to test the resistance between each node. To show there is good contact between the wires and the wafer, resistance should be less than $1M\Omega$. The red wire's resistance with the brown, blue, green, yellow, and orange wires were 0.90 $k\Omega$, 0.90 $k\Omega$, 0.92 $k\Omega$, 1.00 $k\Omega$, and 0.98 $k\Omega$, respectively. The errors for all these measurements were $\pm 0.005k\Omega$ This shows that all the connections were good enough to move on in the experiment. It was noted that the resistances between each node were slowly rising as measurements were being taken but were always well below the $1M\Omega$ limit during the course of the lab.

Using a second silicon wafer, dimensions were recorded. Dial calipers were used to measure a wafer thickness, d, of $0.43 \pm 0.02mm$. The sample was treated as a rectangle, however the real shape of the wafer was closer to a trapezoid. This leads to a width measurement which relatively large error. The width and length of the wafer were $7.0 \pm 1.3mm$ and $18.9 \pm 0.3mm$, respectively.

A current was then applied between nodes 1 and 4 using the power supply. Throughout the experiment, the power delivered across the silicon wafer was kept below 0.1 W. Two DMM's were used to measure the current and voltage across the wafer. The circuit diagram can be seen in Figure 2. The current vs voltage graph obtained can be seen in Figure 3. This figure shows that the semiconductor does not show "ohmic" behavior since the curve is not a straight line. This is because as voltage increases, the temperature of the semicondcutor increases. As temperature increases, resistance decreases and current will be higher. This is shown in Figure 4. Once the voltage goes past around 5 volts, the resistivity steadily declines. This corresponds with a more than linear increase in current.

B. Resistivity and Thermoelectric Effect

To find the resistance of the silicon wafer, using a DMM is not adequate. This is because the DMM will measure the resistance of the chip along with the resistance in the rest of the circuit which includes the soldering joint and

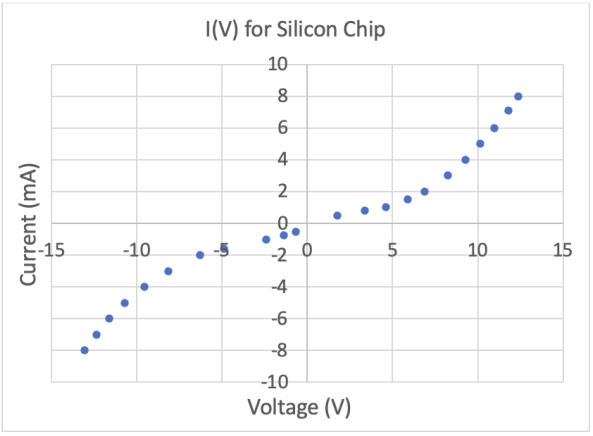

FIG. 3. Current vs Voltage for Silicon Wafer End Nodes

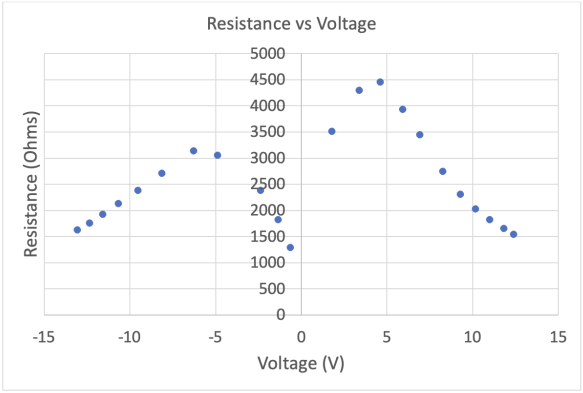

FIG. 4. Resistance vs Voltage for Silicon Wafer End Nodes

measuring equipment. To get a more accurate resistance measurement, the 4-wire method is used.

While applying current of $5.00 \pm 0.05mA$ through the end nodes (1-4), voltage was measured across each pair of inner contacts (2-3 or 5-6). Resistance, R, was then calculated using Ohm's Law. The lead distance between each pair of inner contacts, L, was measured and used to calculate the resistivity, ρ, of the wafer using Eq. 2, where A is the area of the cross section the current goes through. In this experiment A is calculated to be $3.0 \pm 0.6mm^2$.

$$R = \frac{\rho L}{A} \tag{2}$$

These values and the calculated resistivities can be seen in Table I. A typical resistivity value of silicon is 6.40 Ohm-cm [1] so the calculated values fall into accepted values.

The resistance values between nodes 2-3 and 5-6 when measured with a DMM were $1745 \pm 5\Omega$ and $1140 \pm 5\Omega$. The reason these values are much higher than the values obtained using the 4-wire method is because the DMM measures the resistance in the whole circuit which in-

TABLE I. Resistivity Calculation Variables

Nodes	2-3	5-6
Voltage (V)	0.56 ± 0.005	0.59 ± 0.005
Resistance (R)	112.0 ± 1.5	118.0 ± 1.5
Lead Distance (mm)	5.0 ± 0.3	6.0 ± 0.3
Resistivity (Ohm-cm)	6.7 ± 1.4	5.9 ± 1.2
Average Res. (Ohm-cm)	6.3 ± 0.9	

cludes the connections between the indium solder and the silicon wafer.

The "carrier type" of a semiconductor can either be p-type for holes or n-type for electrons. N-type semiconductors are doped in a way where there are excess electrons that move around the semiconductor. In a p-type, there is a lack of electrons so "holes" or positive charges move through the semiconductor. To determine which type the silicon wafer was, the thermoelectric effect was used.

A voltmeter was connected across the two outer nodes. The positive side was connected to the orange wire and the negative side was connected to the blue wire. The hot soldering iron was momentarily brought close to the orange wire contact and the voltage was observed to go negative. This means that there was a build up of positive charges on the blue contact and negative charges on the orange contact. The thermoelectric effect shows that charge carriers will go from the hot side to the cold side of the semiconductor [2]. Therefore, the charge carrier on this silicon wafer were positively charged holes, making this wafer a p-type semiconductor. This was confirmed by moving the soldering iron tip to the blue contact and observing a positive voltage.

C. Hall Effect, Carrier Concentration, and Mobility

The electromagnet was first calibrated with a Gauss meter. This was done by putting the Gauss meter in the correct direction in between the two electromagnets. With the magnet current equal to 0, the Gauss meter was zeroed. Measurements of the magnetic field, B, were then taken at different input current levels. The input current to the magnet never exceeded an absolute value of 3.0 Amps. This calibration can be seen in Figure 5.

This gives us an α for the calibration equation $B = \alpha I_M$ of $100.66 \pm 0.02 mT/A$, where I_M is the input current to the electromagnet [3].

The next step is to figure out which pair of nodes to use for the Hall Effect experiment. When current is being applied across the end nodes, the voltage across the narrow width of the wafer (3-5 or 2-6) should theoretically be 0. However, the nodes are not perfectly in line so there is a small amount of voltage being produced by

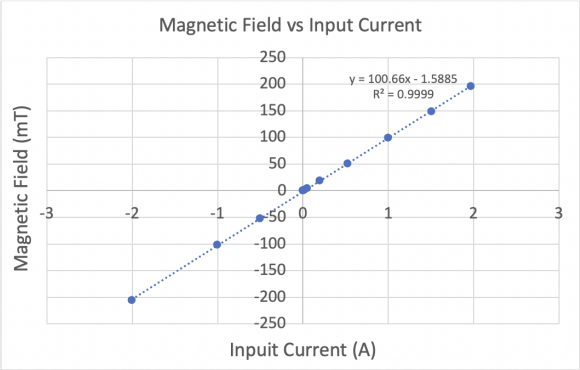

FIG. 5. Magnetic Field vs Input Current for Calibration

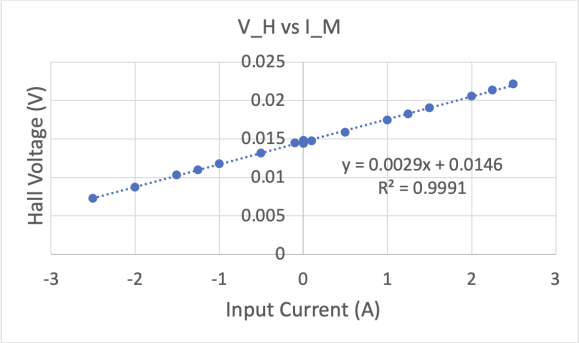

FIG. 6. Hall Voltage vs Input Current

the current flow. A current of $6.00 \pm 0.05 mA$ was applied from the orange wire to the blue wire. The voltage from yellow to red was measured to be $-0.0185 \pm 0.0005 V$ and the voltage from green to brown was measured to be $-0.7350 \pm 0.0005 V$. This shows that the yellow to red connection (5-3) was more normal to the current flow and was chosen as the Hall pair to measure during the next part of the experiment.

The silicon wafer was placed in between the magnet poles, equidistant from the two pole faces. The wafer was oriented in a manner than the magnetic field, input current, and Hall effect voltage pair are all normal to each other. The current going into the wafer was set to have an initial value of $0.004020 \pm 0.000005 A$. The Hall voltage, V_H, and sample current, I_S, were then measured as a function of the magnet input current, I_M. This was done in both directions by reversing the current through the electromagnet. From this data, Figure 6 was obtained and subsequently Figure 7 was made by multiplying the x-axis by the previously found α value. It is important to note Hall Voltage doesnt go through the origin of either graph due to the small offset in distance of the Hall pair found in the previous section. When the voltage produced by the Hall effect is 0, there is a voltage being produced by the current flowing in the wafer.

Figure 8 shows the direction of the magnetic field and

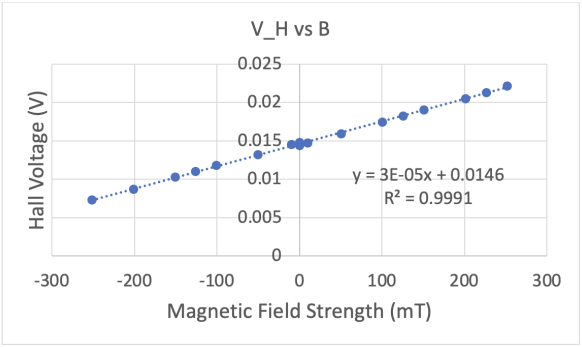

FIG. 7. Hall Voltage vs Magnetic Field Strength

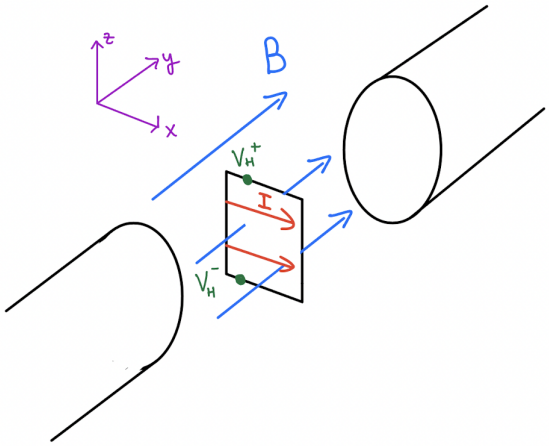

FIG. 8. Vector Directions for Hall Experiment

the current along with the resulting Hall voltage. The direction of the Lorentz force on positive charges moving in the direction of the current with a magnetic field in the shown direction would be applied to the positive z axis. This is what was observed, further proving the wafer is a p-type semiconductor. If the carriers were electrons, the particle would be going in the negative x direction and a Lorentz force would push the electron upward creating an opposite voltage to what was observed.

Using Equation 3, where e is the charge of an electron, the carrier density, n, was measured to be $(1.90 \pm 0.10) * 10^{15} \frac{carriers}{cm^3}$. The value of $\frac{dV_H(B)}{dB}$ was obtained from the slope of Figure 7 to equal $0.02912 \pm 0.00009 V/T$. The National Institute of Standards and Technology (NIST) lists that the carrier density of p-type silicon is commonly in between 10^{13} and $3 * 10^{18}$ so the found value is within typical values [4].

$$V_H = \frac{BI_S}{ned} \tag{3}$$

Then, using Equation cm, the carrier mobility is found to be $520 \pm 80 \frac{cm^2}{V-s}$. Using BYU's online resistance and mobility calculator gives an expected carrier mobility value of $412.2 \frac{cm^2}{V-s}$ at the calculated carrier density [5]. While this is not within the calculated error, is it on the same order of magnitude of the calculated value.

$$\rho = \frac{1}{ne\mu} \tag{4}$$

SUMMARY

Table II shows the values for resistivity, carrier concentration, and carrier mobility found in the experiment. Typical values for these are $7.97 Ohm - cm$, within 10^{13} and $3 * 10^{18} cm^{-3}$, and $412.2 cm^{-2} V^{-1} s^{-1}$ [5] [4]. The only value found that is definitely within typical values is the carrier concentration but it is important to note that the citation used for the other values does not provide a range of possible values but rather a single output from an equation. Small errors in the set up are most likely what led to the other found values being slightly off from typical values for a p-type silicon semiconductor.

It is important to note that mobility decreases with respect to an increase in concentration. The largest of source of error in this experiment most likely comes from measurement of the cross sectional area since the specimen was not a perfect rectangle. Another source of error occured when measuring the Hall Effect since the specimen current was steadily decreasing over time which affects the caculated carrier concentration and mobility.

TABLE II. Final Measured Values for Hall Effect Experiment.

Resistivity, ρ $(\Omega - cm)$	6.3 ± 0.9
Carrier Concentration, n (cm^{-3})	$(1.90 \pm 0.10) * 10^{15}$
Carrier Mobility, μ $(\frac{cm^2}{V-s})$	520 ± 80

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[1] "2.4: Semiconductors," *LibreTexts,*

https://chem.libretexts.org/Bookshelves
[2] "1.1 Fundamentals of Thermoelectrics," *H. Karamitaheri,* https://www.iue.tuwien.ac.at/phd/karamitaheri/node9.html
[3] "Introductory Physics Lab," https://web.northeastern.edu/ipl/data-analysis/straight-line-fit/
[4] "Sheng Li," https://nvlpubs.nist.gov/nistpubs
[5] "Resistivity and Mobility Calculator," https://cleanroom.byu.edu/resistivitycal